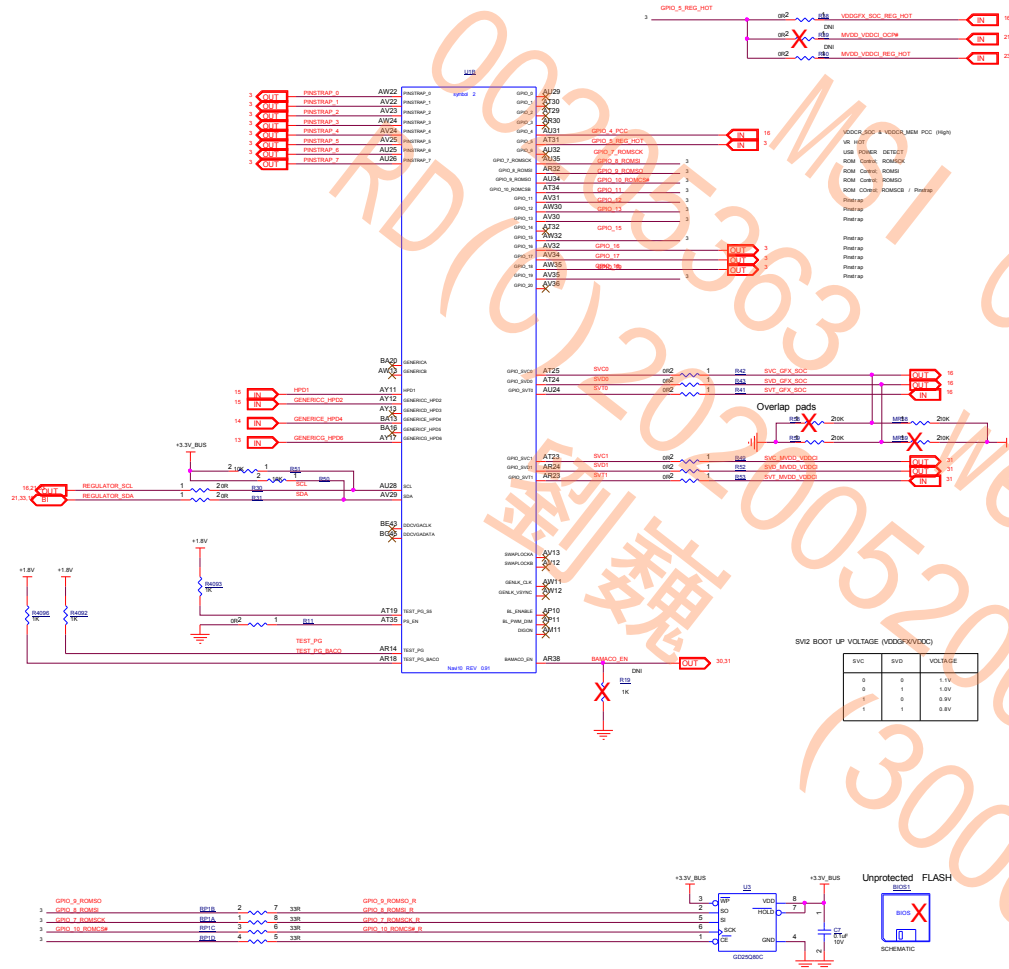


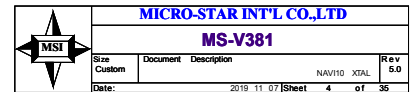
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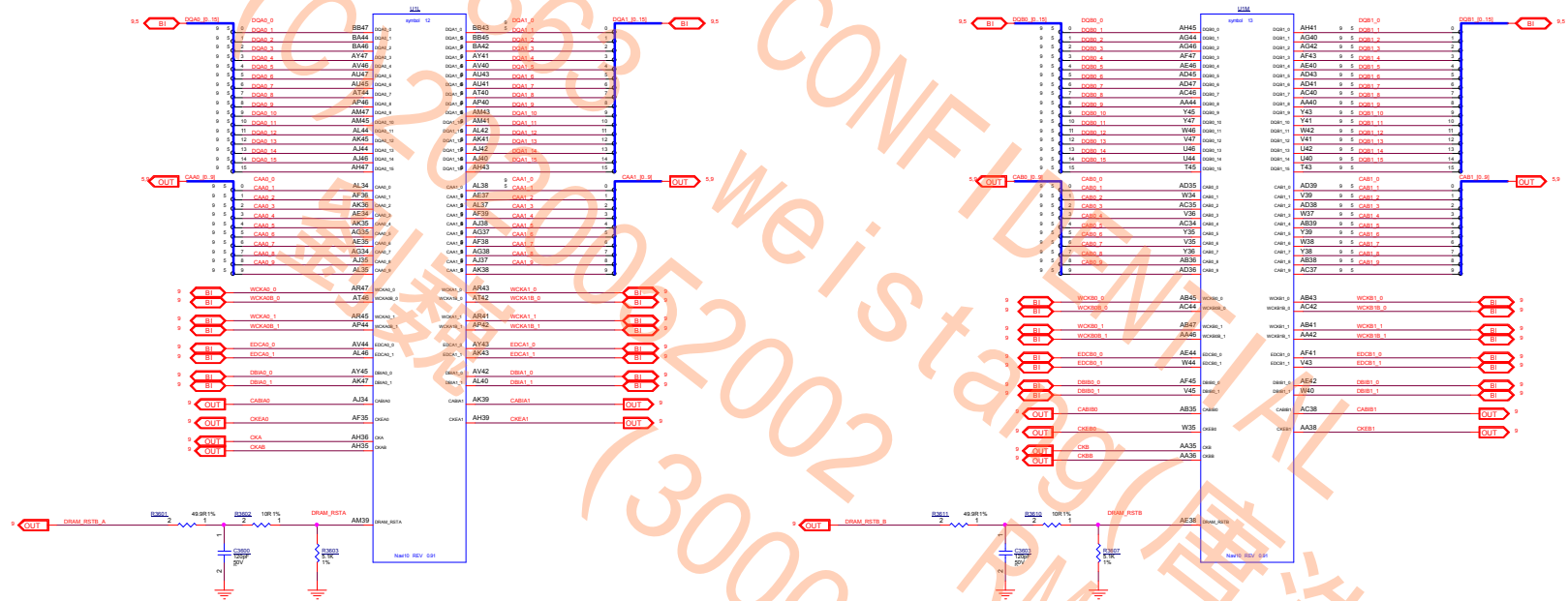
SHEET NO.	SHEET NAME	SHEET NO.	SHEET NAME
1	TOC	26	SMALL RAIL REGULATORS
2	NAV110 PCIe Interface	27	NAV110 DECAPS
3	NAV110 GPIOs	28	NAV110 POWER
4	NAV110 XTAL	29	NAV110 GND
5	NAV110 MEM CHAB	30	POWER MANAGEMENT
6	NAV110 MEM CHCD	31	SVR2 & BAMACO
7	NAV110 MEM CHEF	32	MECHANICAL & THERMAL
8	NAV110 MEM CHGH	33	DEBUG
9	GDOR8 MEM CHAB	34	BLOCK DIAGRAM
10	GDOR8 MEM CHCD	35	REVISION HISTORY
11	GDOR8 MEM CHEF		
12	GDOR8 MEM CHGH		
13	NAV110 TMDPA - DP		
14	NAV110 TMDPC - HDMI		
15	NAV110 TMDPEF - DP DP		
16	GFX & SOC CONTROLLER		
17	VDDCR_GFX PHASES 2 and 5		
18	VDDCR_GFX PHASES 1 and 4		
19	VDDCR_GFX PHASES 3 and 7		
20	VDDCR_GFX PHASES 6 and VDDCR_SOC		
21	MVDD_VDDCI CONTROLLER		
22	REG MVDD		
23	REG VDDCI		
24	REG 0.75V		
25	REG 1.8V		

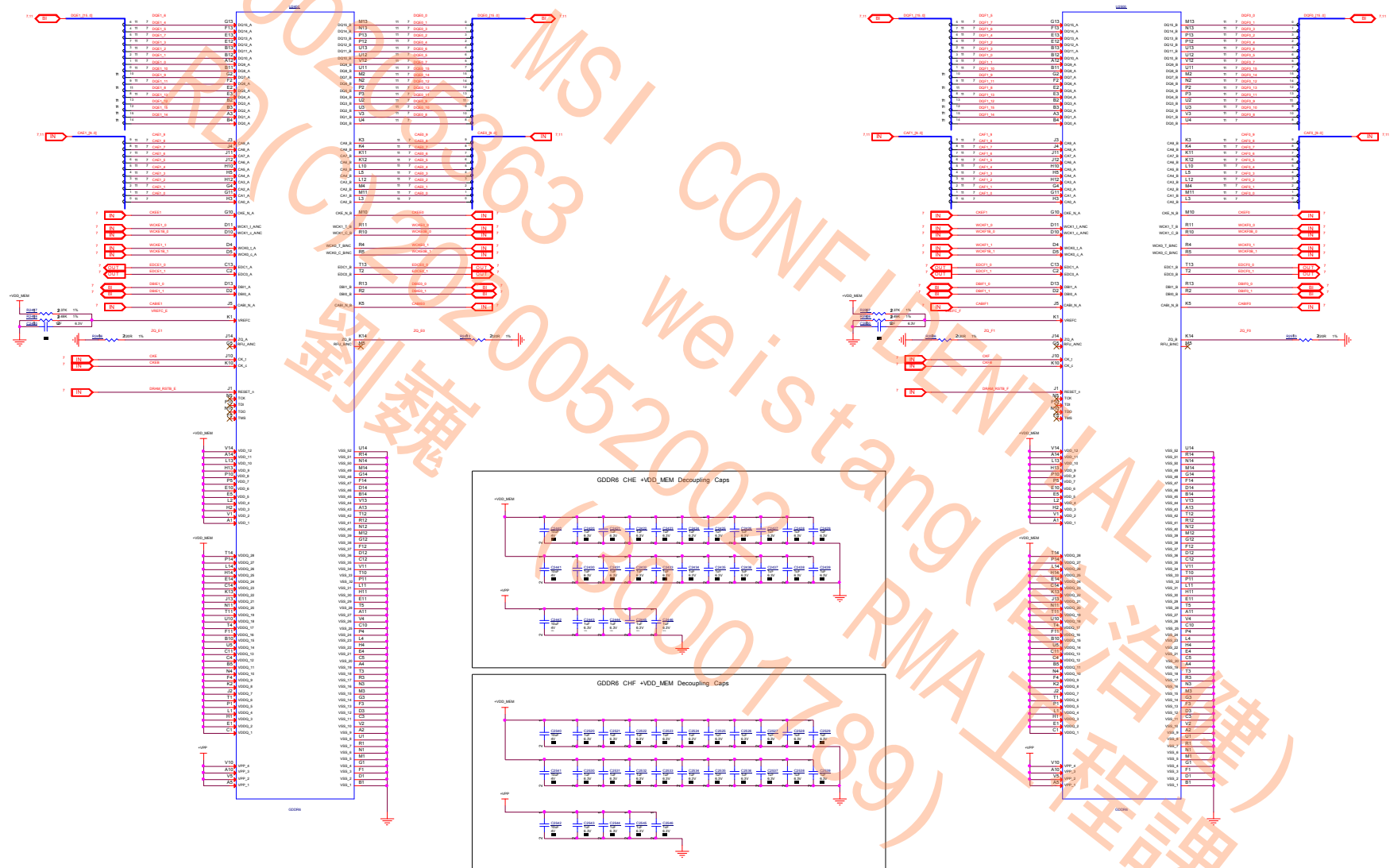


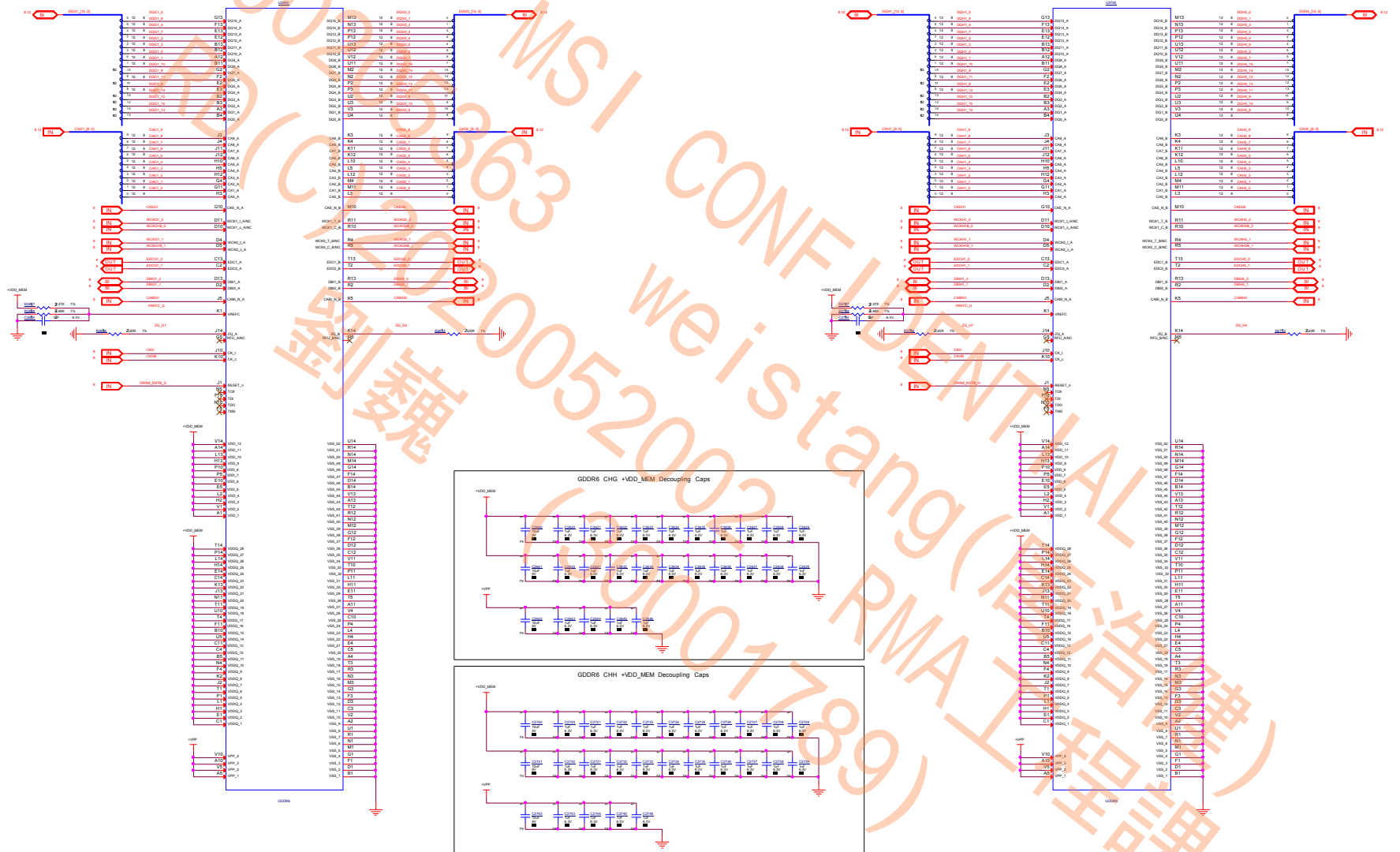
Note: Internal PUPD at GPIO pad is ~40k strength in 14nm design spec

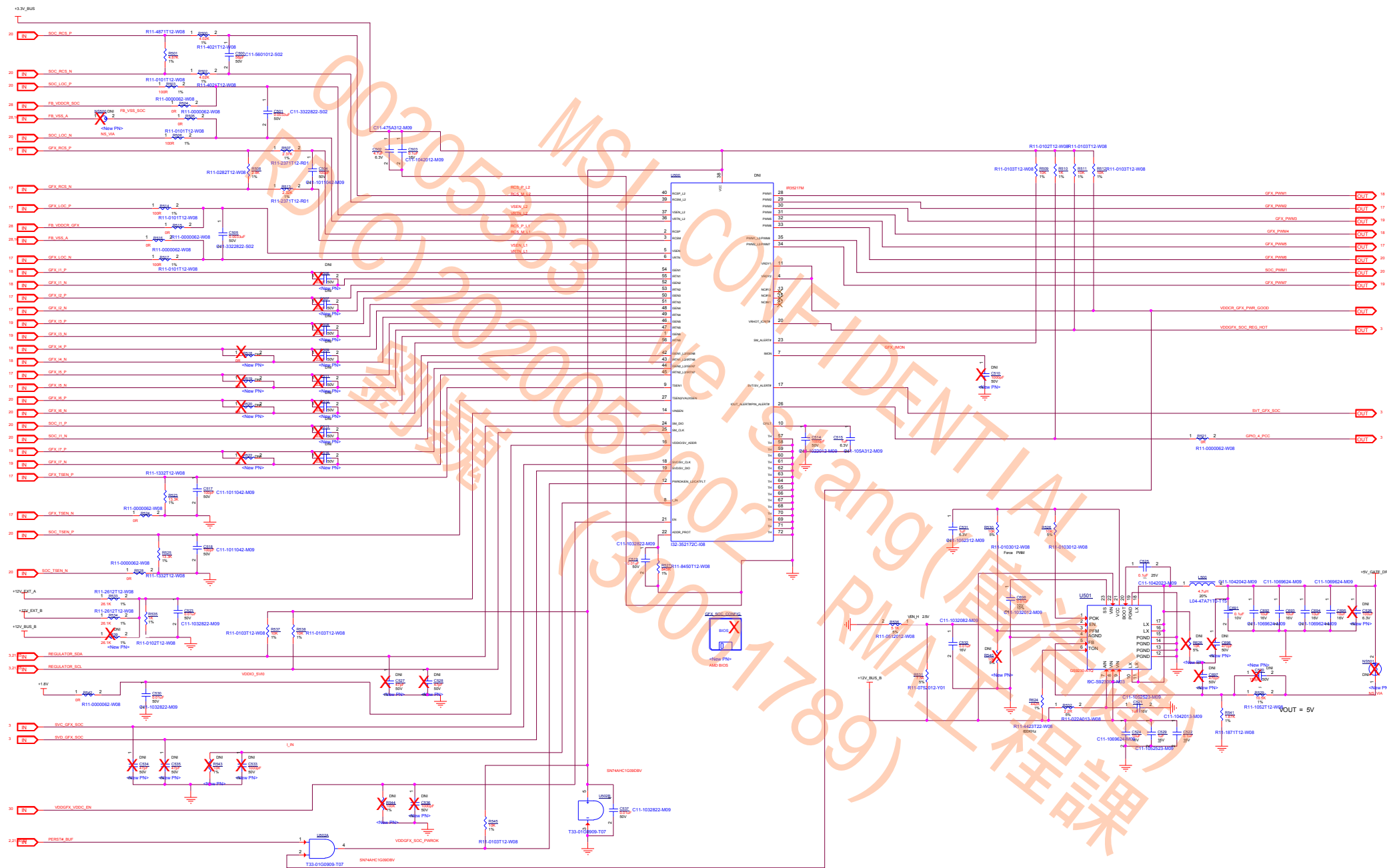
User	Internal Default Value	Definition
BIF	0	STRAP_BIF_GEN4_DIS_A 0: BIF GEN4 not supported 1: BIF GEN4 not supported
	0	PINSTRAP_BIF_CLK_PM_EN 0: CLKSTRAP power management capability is disabled 1: CLKSTRAP power management capability is enabled
	0	PINSTRAP_BIF_IC_TX_SWING 0: VDDA converter capability is disabled 1: The device will be equipped on the system's VGA controller
DCE	0	PINSTRAP_BIF_VGA_DIS 0: VGA controller capability is disabled 1: The device will be equipped on the system's VGA controller
	0	PINSTRAP_AUD_PORT_CONN[2:0] Number of audio-capable display outputs 0: 0 endpoints connected 1: 1 endpoint connected 2: 2 endpoints connected 3: 3 endpoints connected 4: 4 endpoints connected
	0	PINSTRAP_AUD[1:0] 1: Audio for DisplayPort only 2: Audio for DisplayPort and HDMI if design is selected 3: Audio for DisplayPort and native HDMI
Platform	0	GPIO_16 0: 0 endpoints connected 1: 1 endpoint connected 2: 2 endpoints connected 3: 3 endpoints connected 4: 4 endpoints connected
	0	GPIO_17 0: 0 endpoints connected 1: 1 endpoint connected 2: 2 endpoints connected 3: 3 endpoints connected 4: 4 endpoints connected
	0	GPIO_18 0: 0 endpoints connected 1: 1 endpoint connected 2: 2 endpoints connected 3: 3 endpoints connected 4: 4 endpoints connected
SMU	1	PINSTRAP_2 0: 0 endpoints connected 1: 1 endpoint connected 2: 2 endpoints connected 3: 3 endpoints connected 4: 4 endpoints connected
	0	PINSTRAP_3 0: 0 endpoints connected 1: 1 endpoint connected 2: 2 endpoints connected 3: 3 endpoints connected 4: 4 endpoints connected
	1	PINSTRAP_4 0: 0 endpoints connected 1: 1 endpoint connected 2: 2 endpoints connected 3: 3 endpoints connected 4: 4 endpoints connected
SMU	0	GPIO_16 0: 0 endpoints connected 1: 1 endpoint connected 2: 2 endpoints connected 3: 3 endpoints connected 4: 4 endpoints connected
	0	GPIO_17 0: 0 endpoints connected 1: 1 endpoint connected 2: 2 endpoints connected 3: 3 endpoints connected 4: 4 endpoints connected
	1	GPIO_18 0: 0 endpoints connected 1: 1 endpoint connected 2: 2 endpoints connected 3: 3 endpoints connected 4: 4 endpoints connected

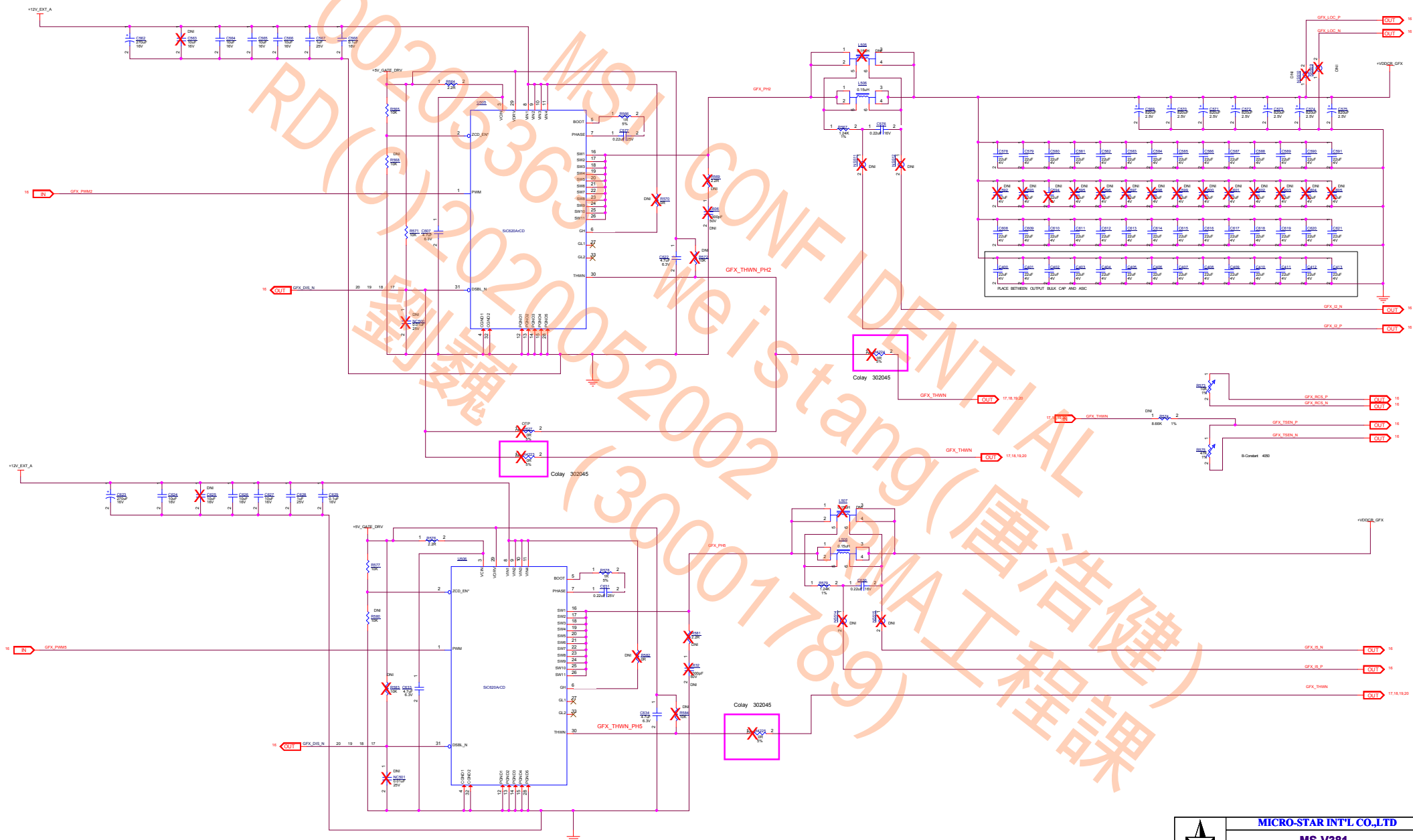


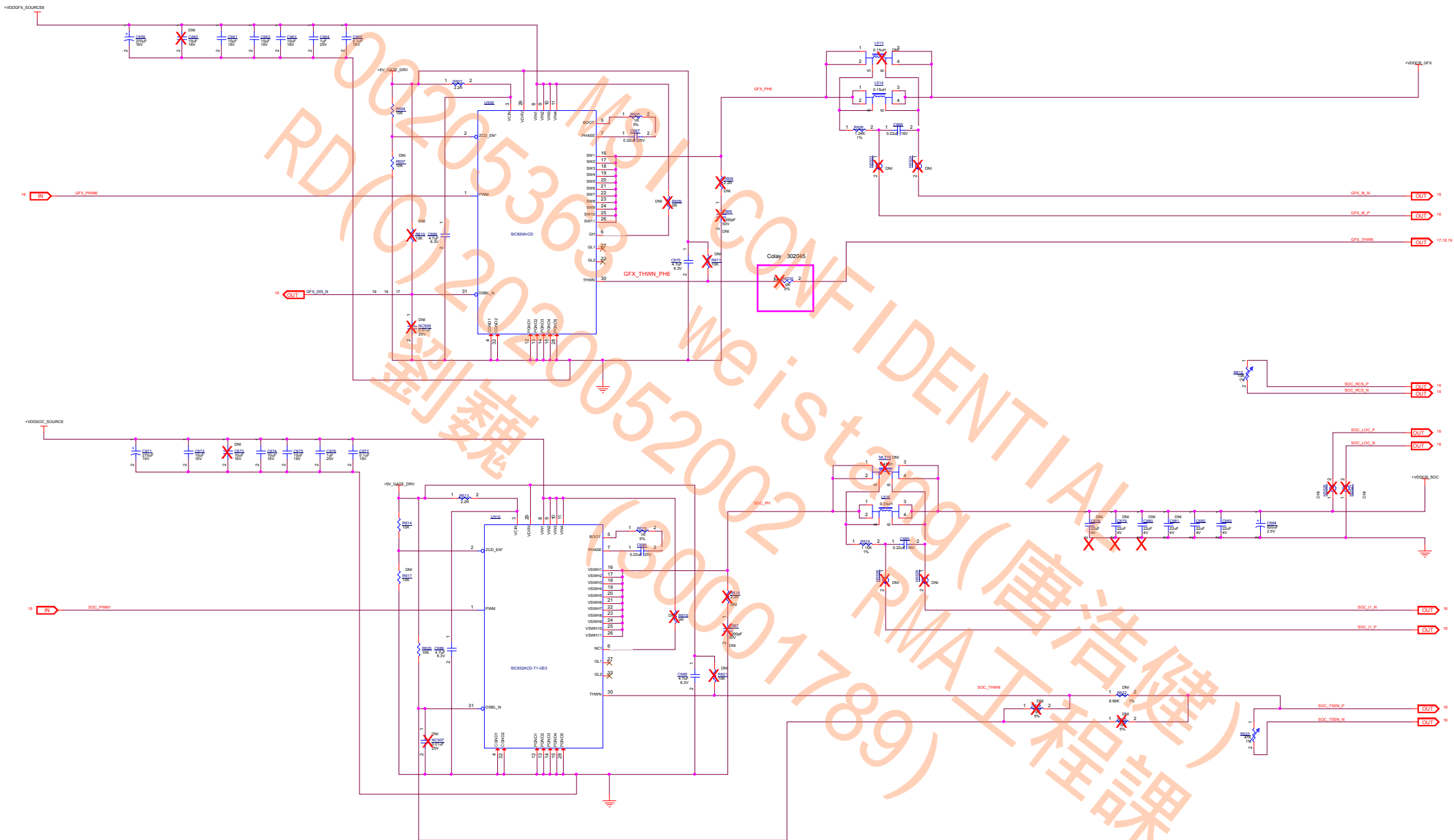


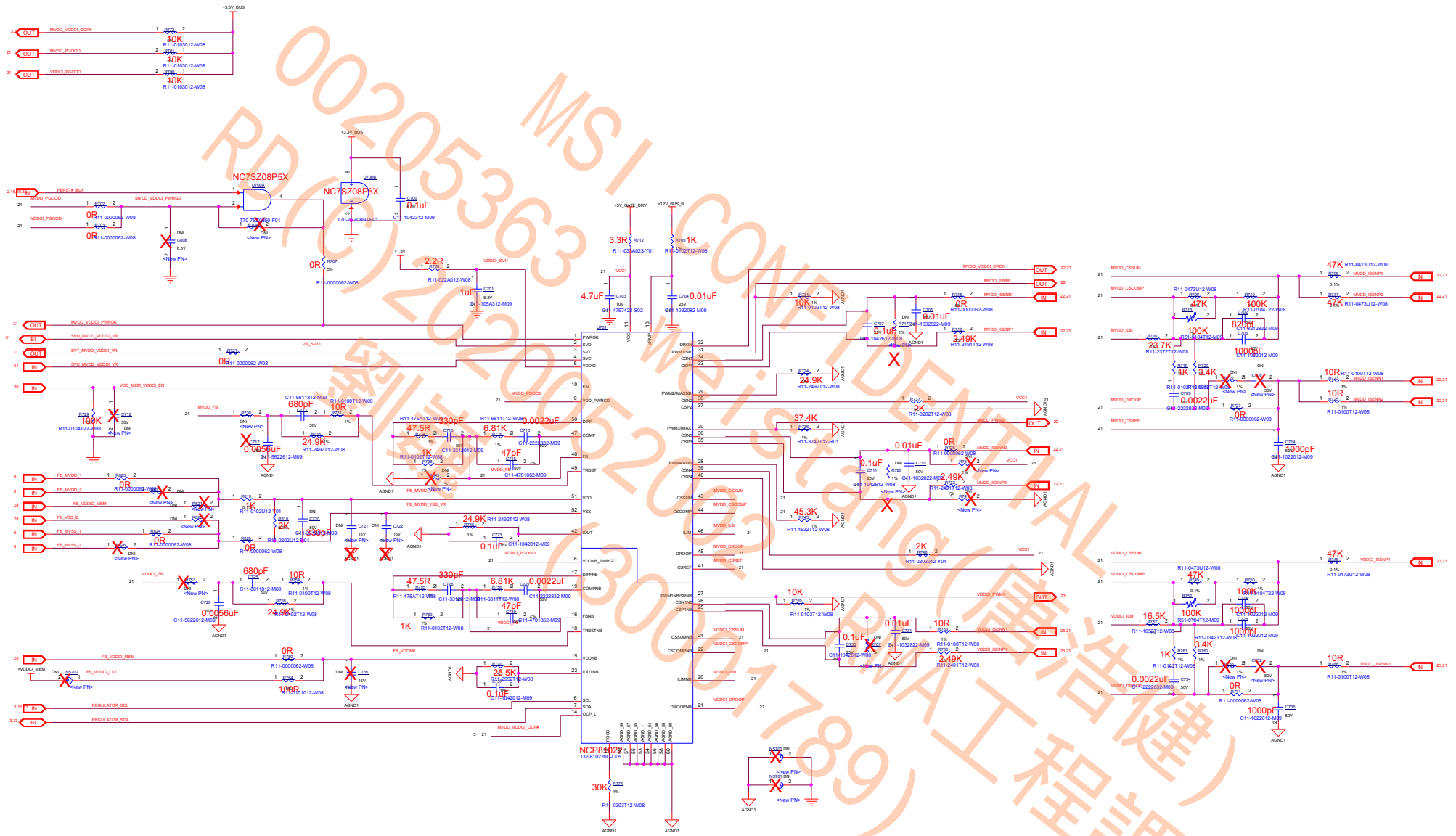


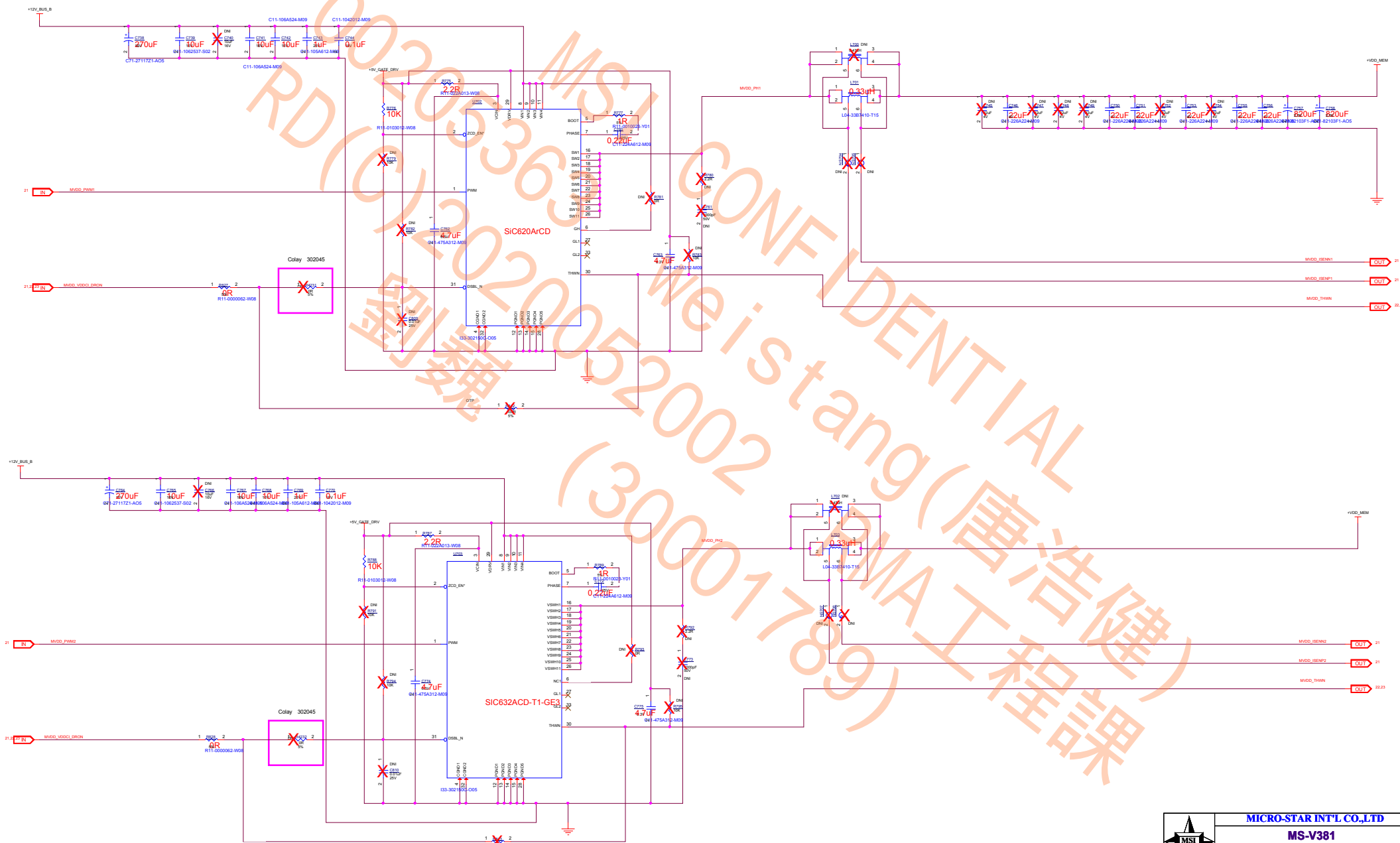


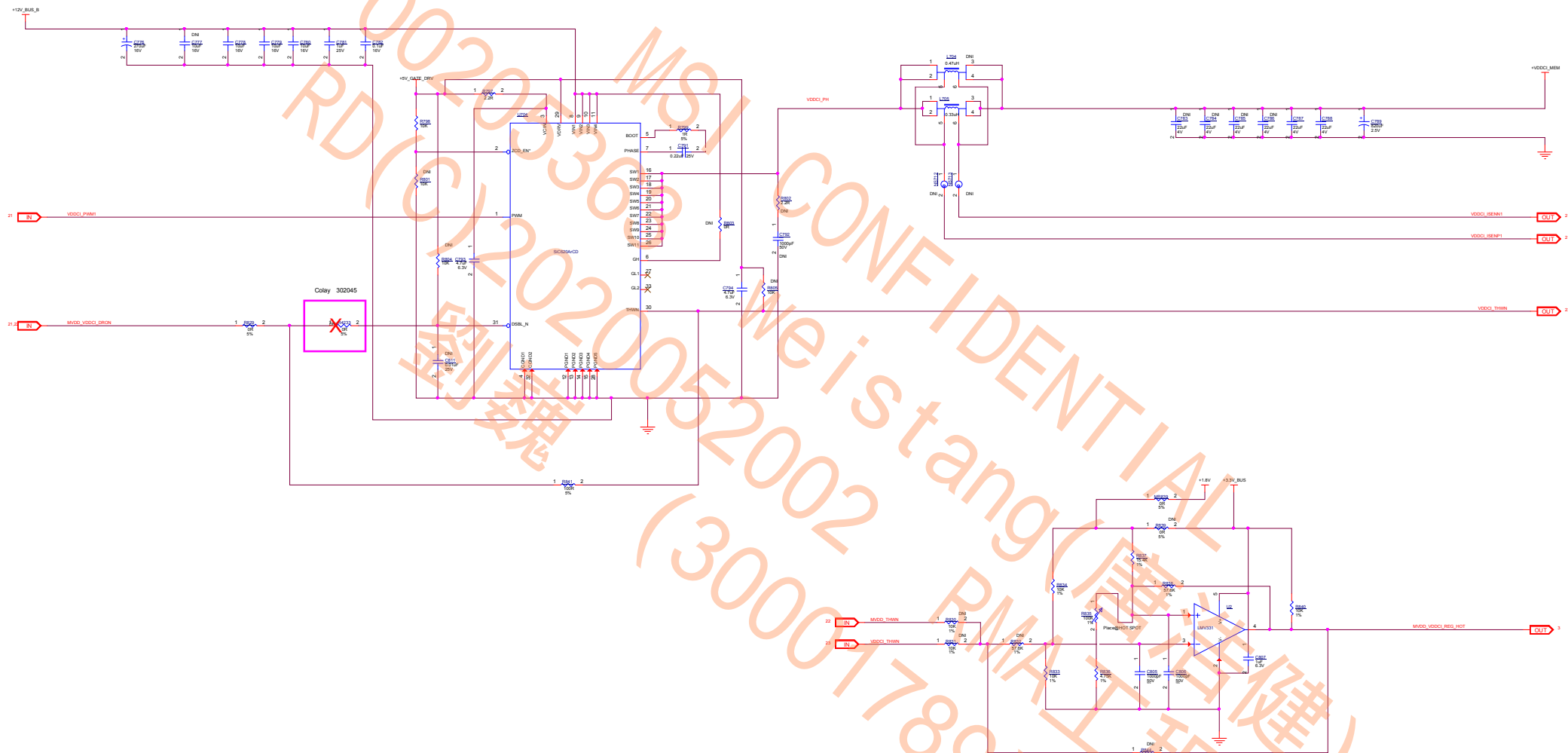


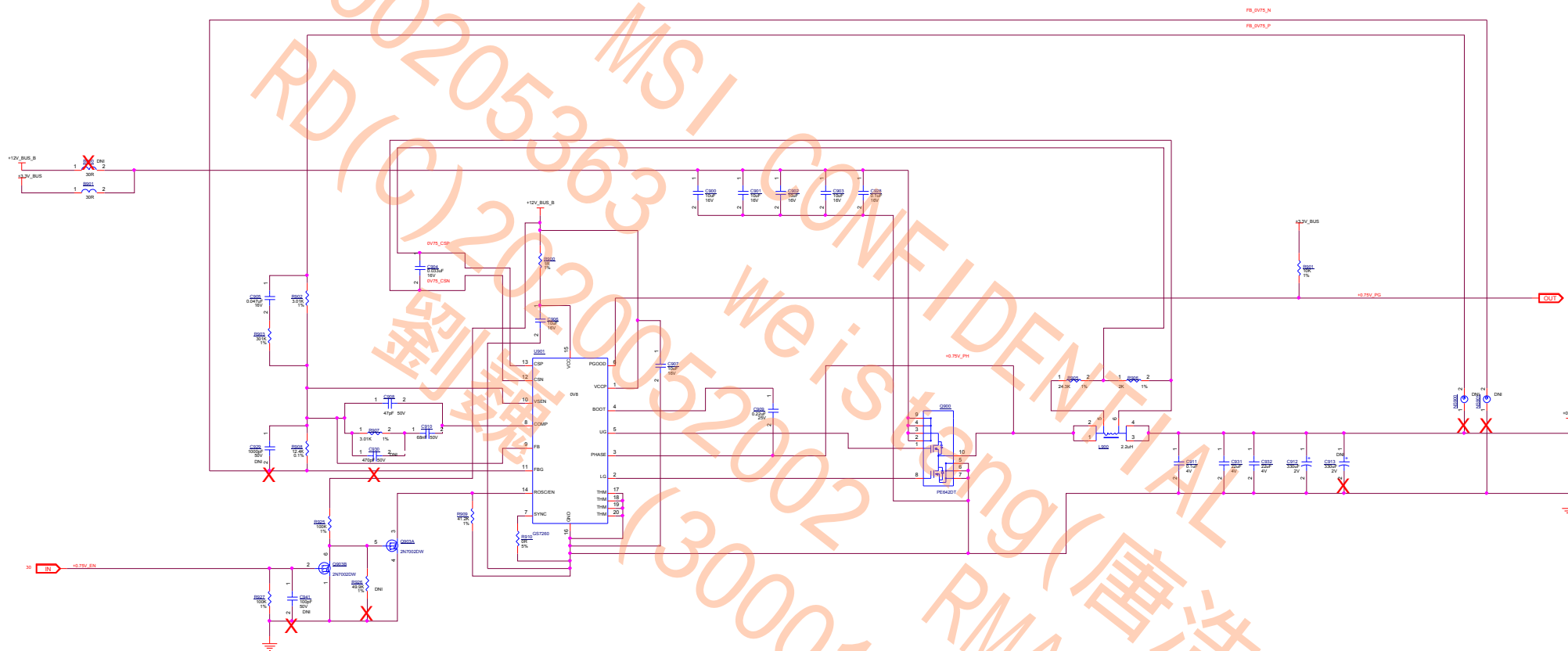






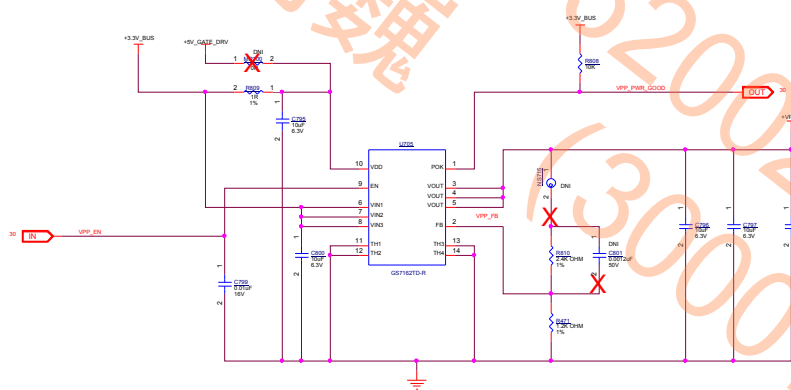
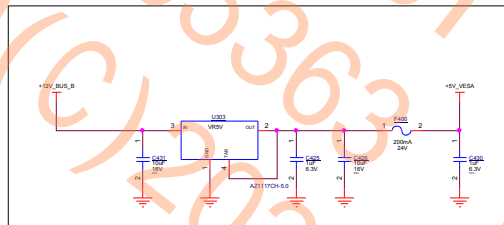


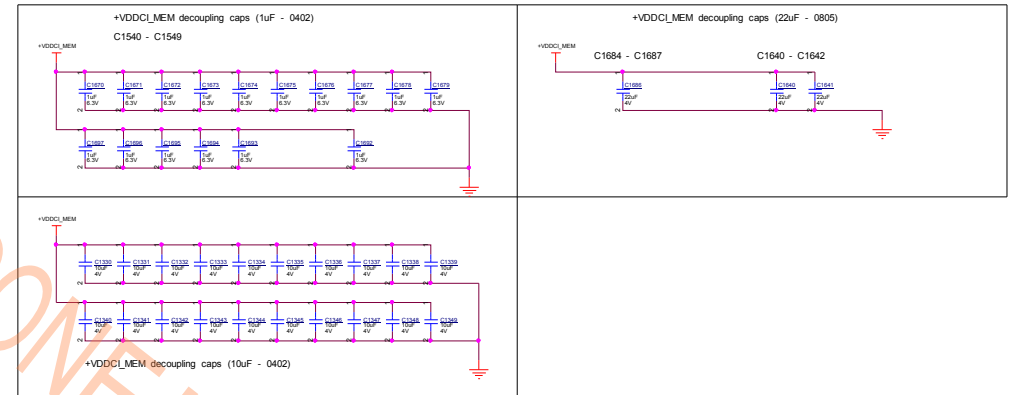
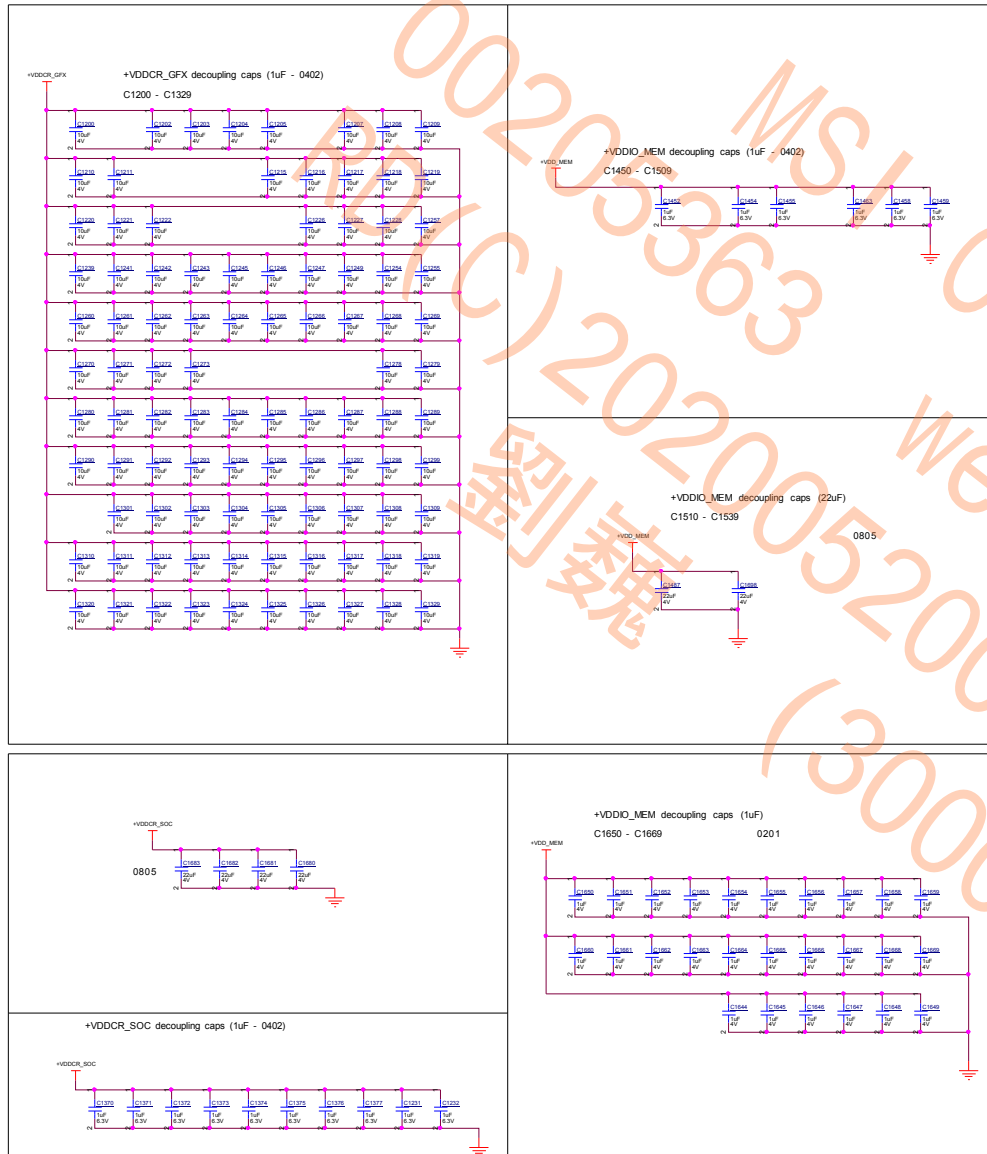


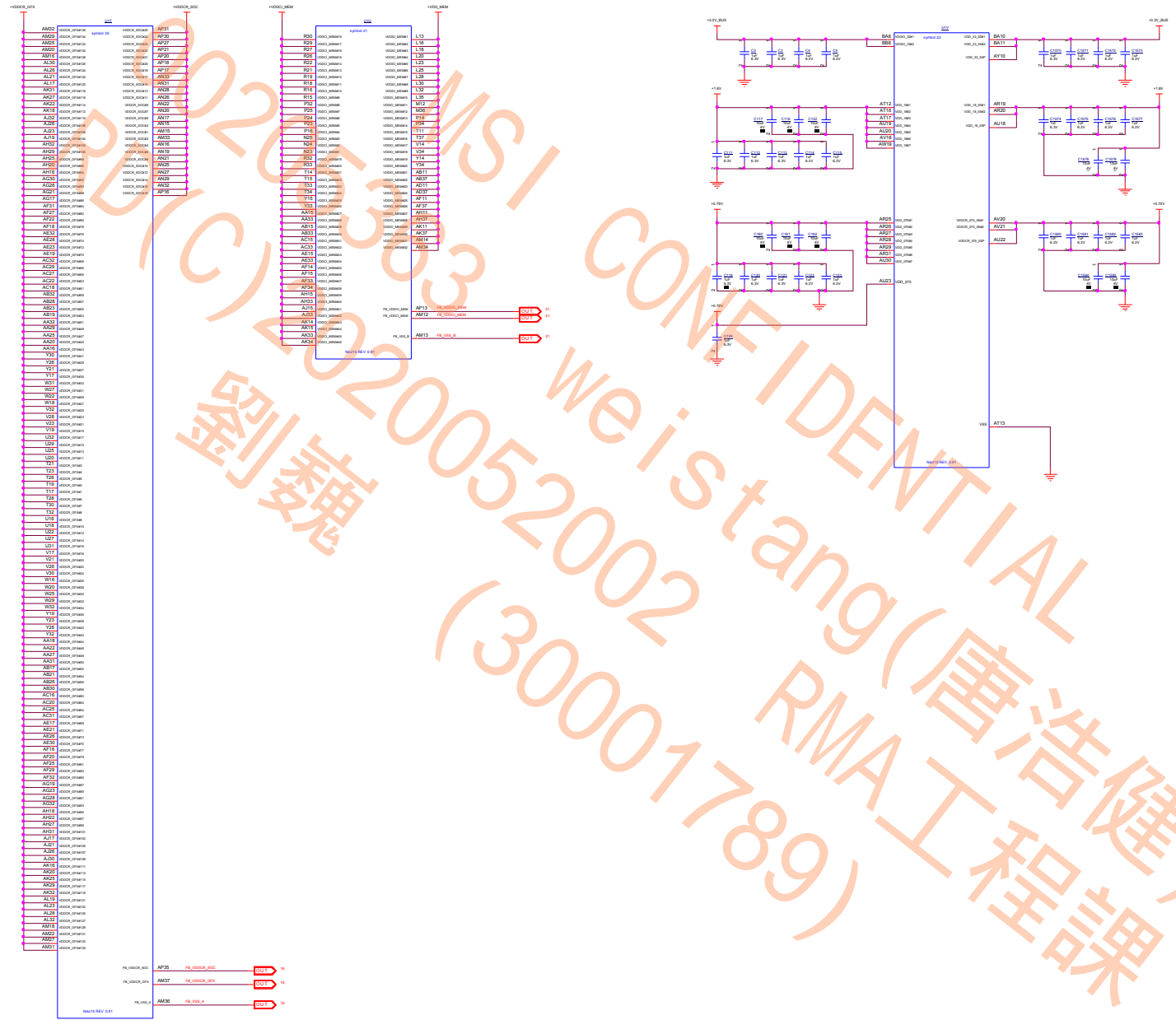


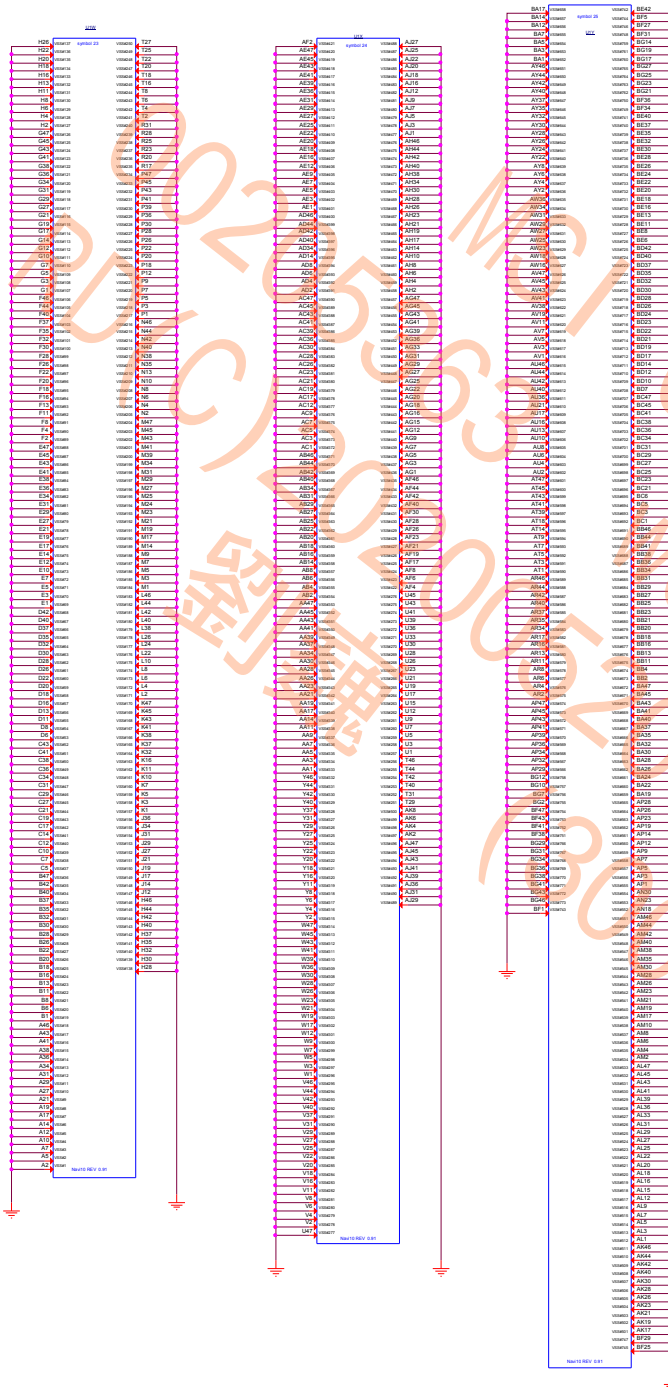


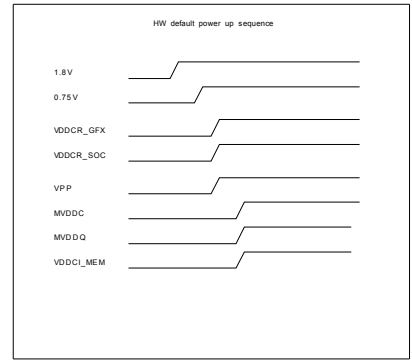
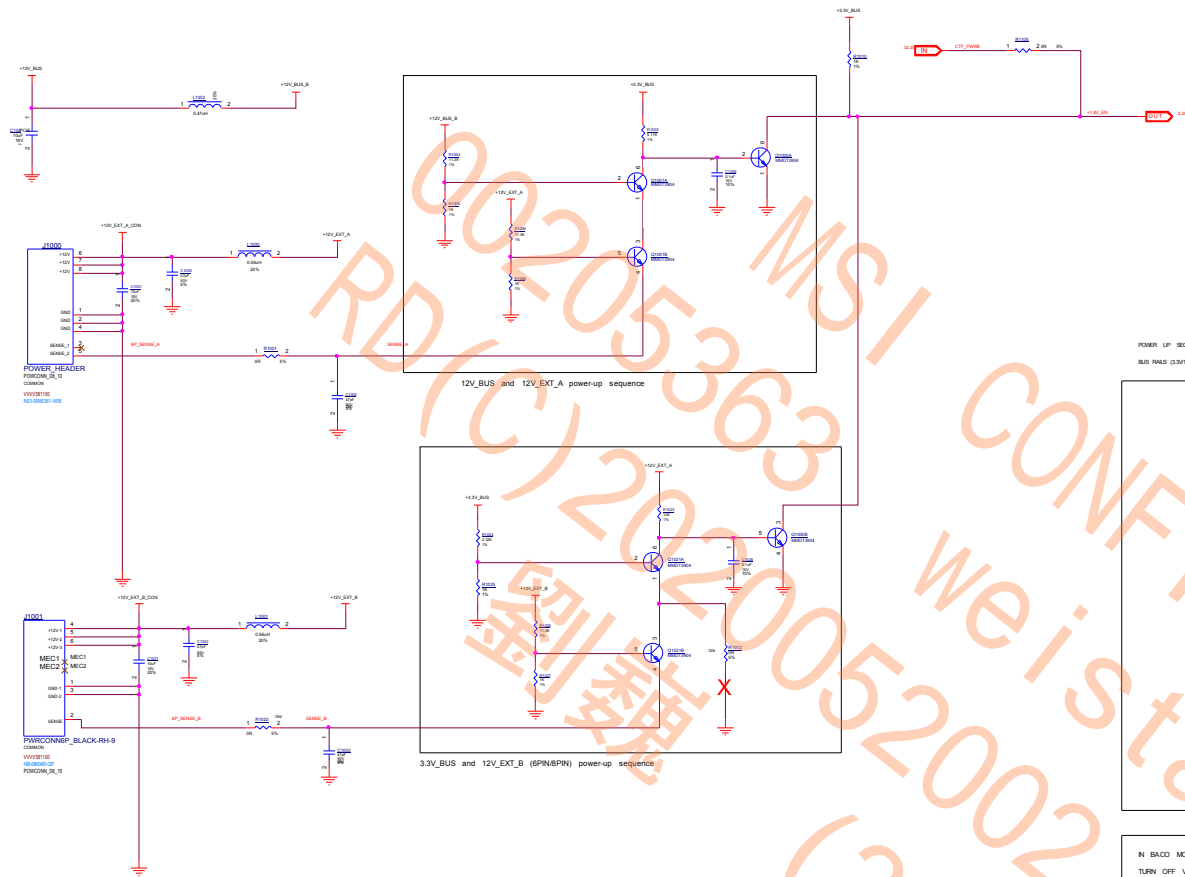
REGULATOR FOR +5V RAILS
I_{OUT} = 50mA



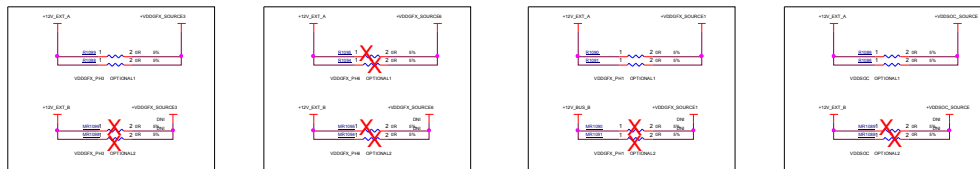
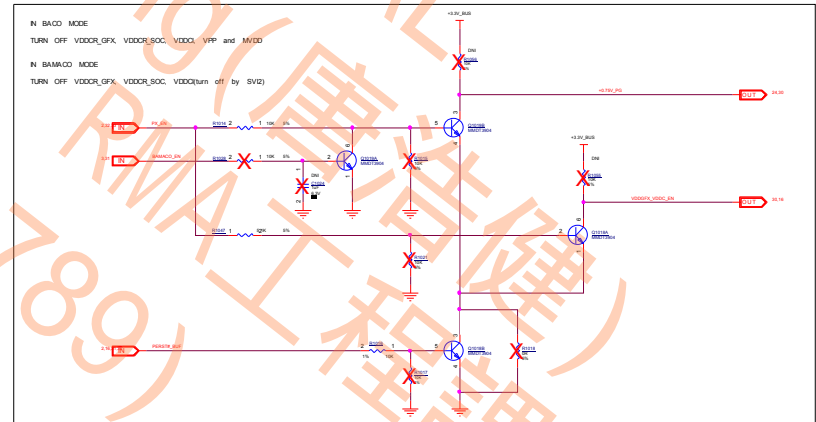
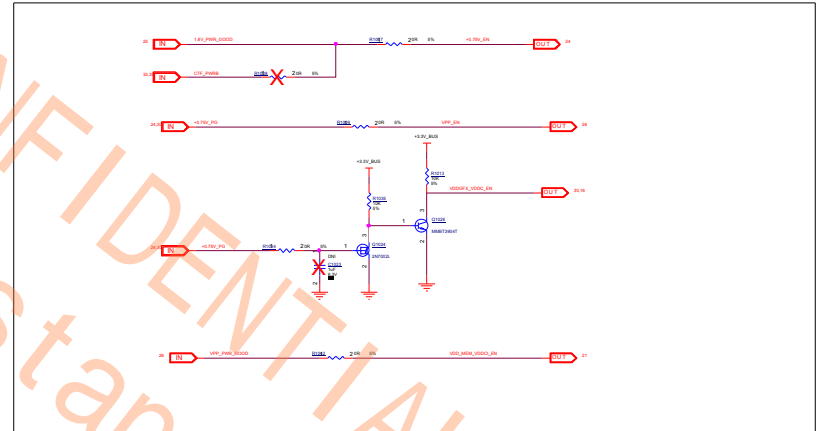


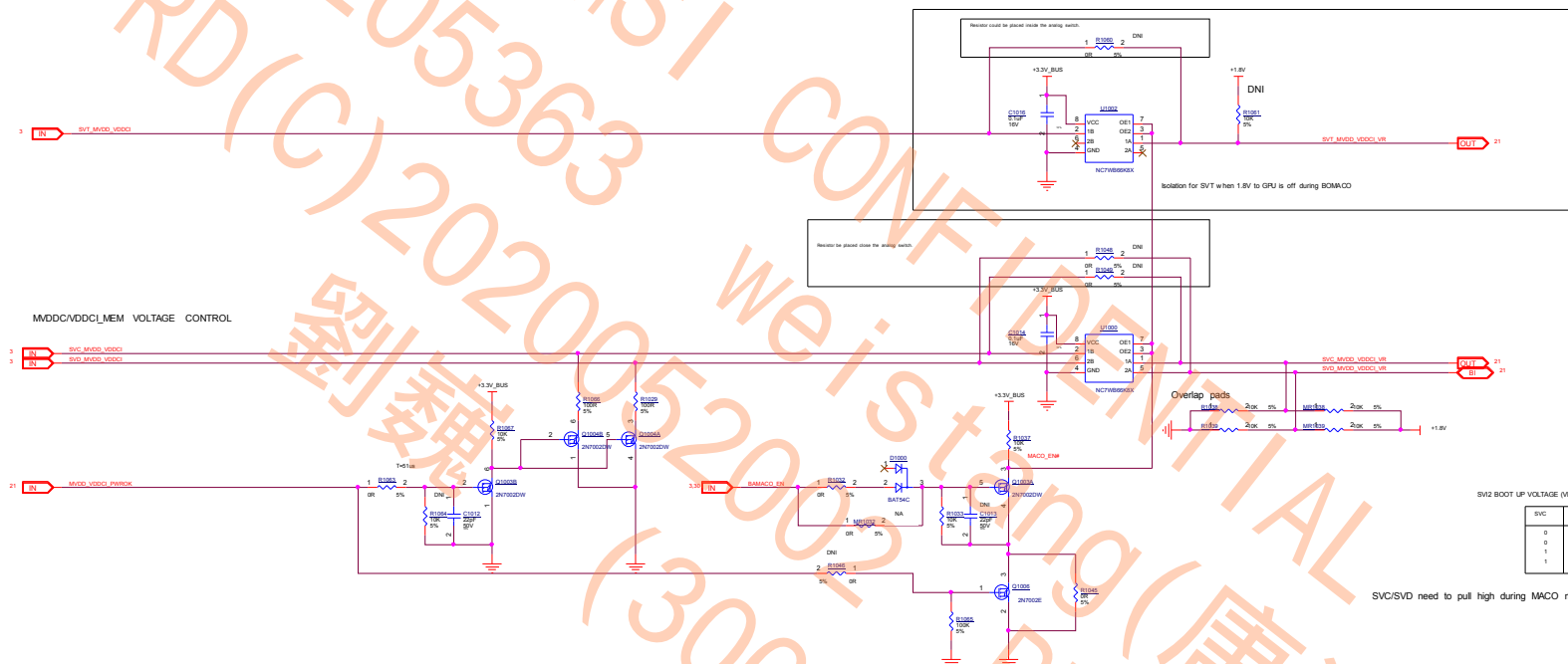






POWER UP SEQUENCE
 BUS RAILS (3.3V/1.2V UP) → +1.8V → 0.75V → VDDCR_GFX/VDDCR_SOC
 → VPP → VDDCI_MEM

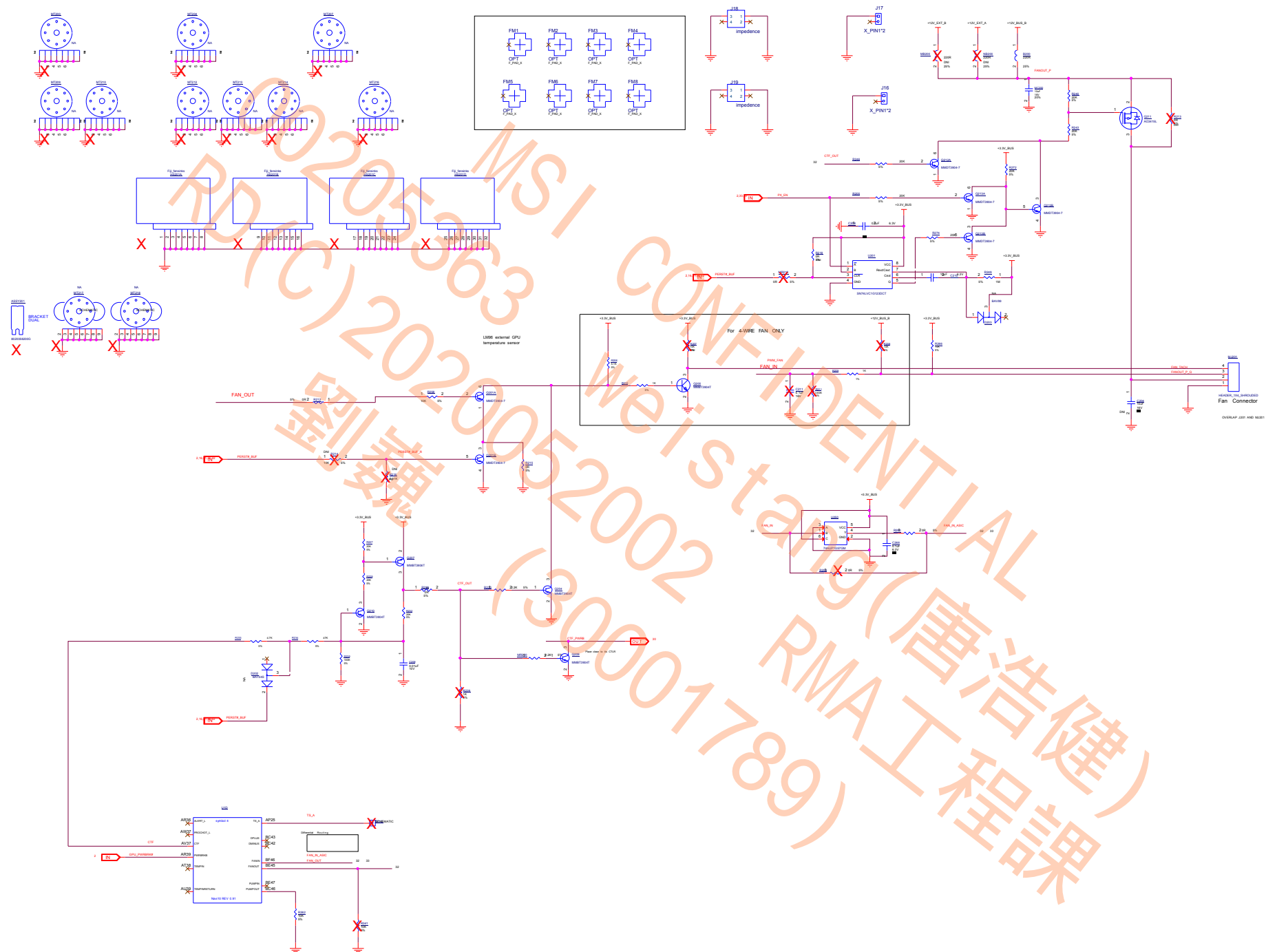


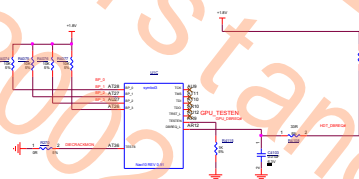
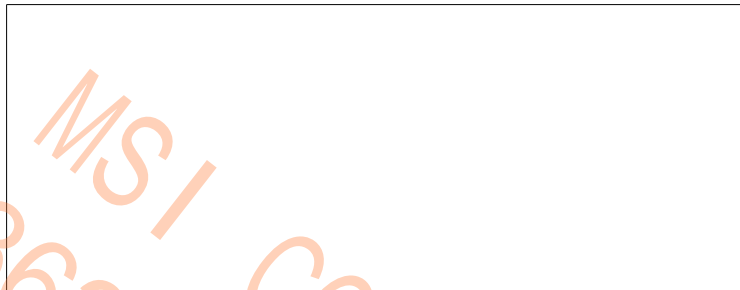
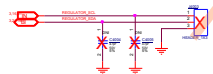


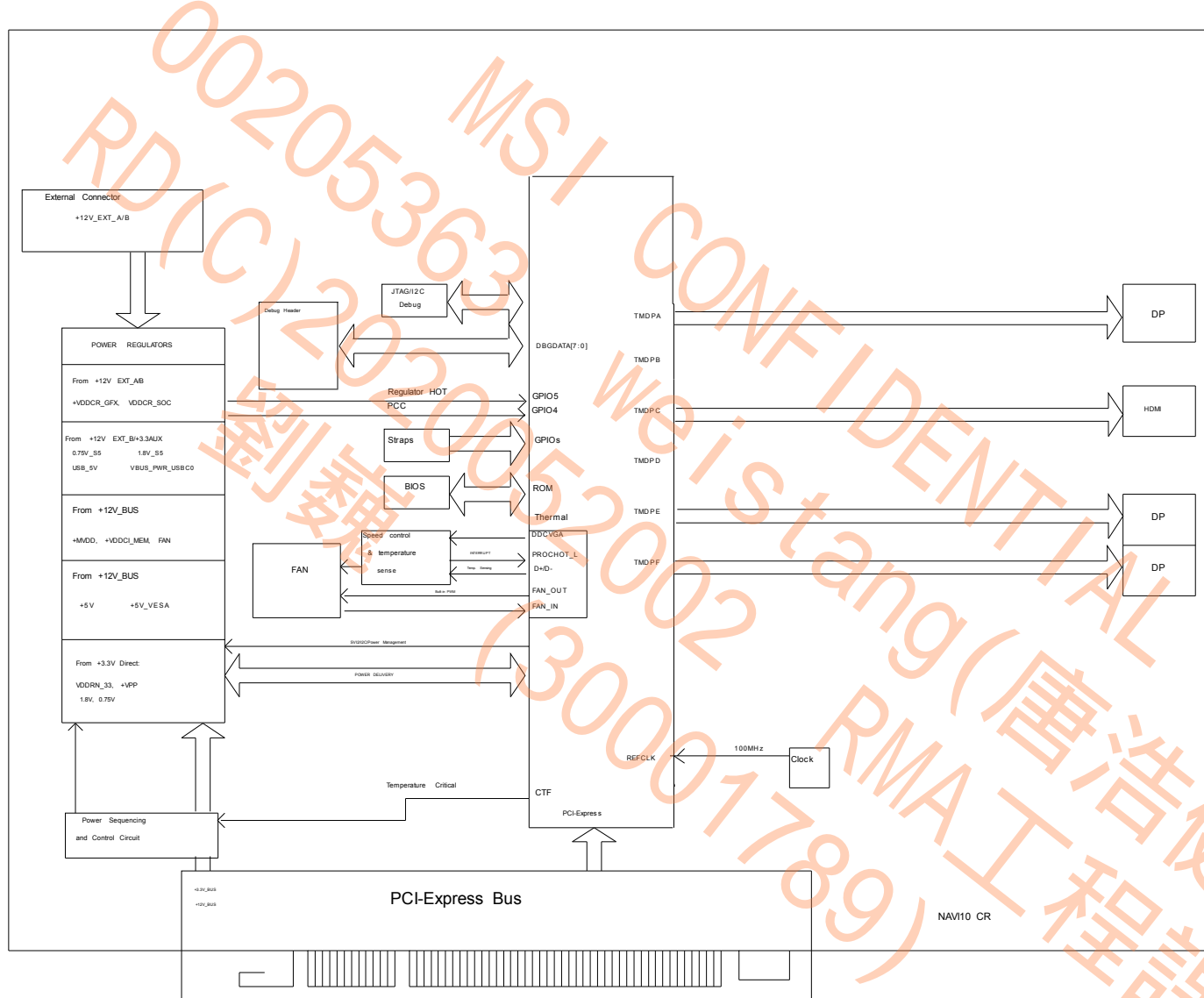
SVT2 BOOT UP VOLTAGE (VDDQ_MEM/MVDD)

SVC	SVD	VOLTAGE
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

SVC/SVD need to pull high during MACO mode









TITLE:

NAVI10 G6X16mode DP DP HDMI DP

DOCUMENT NUMBER:

105_D199xxx_008

DATE:

Fri Jun 21 03:44:58 2019

SHEET NUMBER

35

OF

3

REV: 1.00

REVISION HISTORY

ENGINEER:

Peak, Dong

NOTES :

NOTE

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No.669, HUANKE ROAD
SHANGHAI, CHINA 201203

SCH Rev	PCB Rev	Date	REVISION DESCRIPTION
1	-00A	FEB 11 2019	-00A schematics
2	-00B	AUG 27 2019	ADD PULL HIGH ON THE PWRPWRB
			2019_11_07 GFX_MEM_SOC_VDDCI Co-Lay 302045 and Power PIN fix to 8+6 reverse type Only 2019_11_11 Add Fan_IN output back Page 32, Change Footprint con_dp_astron_r6890020_tab > con_tab , edgecon_pci_express_gen4_16 > edgecon_16 , Remove MT203, MT 211, MT208 Screw Hole 2019_11_14 add Cross Light point , Remove Page 2 TP detect point, Remove lightbar header, Remove CTF & J4100 debug Pin